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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,880	06/20/2003	Kelvin S. Vartti	RA 5614	6661

27516 7590 11/28/2005

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EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,880	VARTTI ET AL.	
	Examiner	Art Unit	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-22 are presented for examination. This office action is in response to the amendment filed on 10/13/2005.

2. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

Specification

3. The disclosure is objected to because of the following informalities:

It appears that "10/600,218" should be changed to --10/600,205—in page 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1, 6-8, and 19-22 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (AAPA) pages 1-3.

As to claim 1, AAPA discloses for use in a data processing system having a memory coupled to multiple requesters (Page 1 lines 26-30) , a memory coherency system (page 2 line 23), comprising: a memory circuit (page 1 line 30) coupled to provide a copy of requested data from the memory to a first requester (Page 2 line 24),

and to initiate invalidation operations (pag2 lines 26-30) to invalidate all read-only copies of the requested data that are stored by one or more other requesters (page 2 line 26); and a circuit (page 2 line 23, cache coherency and page 3 line 13, logic and line 16, methodology) included within the first requester and responsively coupled to the memory circuit to execute an instruction that causes the first requester to temporarily enter a stalled state (pag2 lines 24-30, "delaying processing" and "invalidating old copies of data before data is provided to an IP" read on this limitation0 until all of the invalidation operations have been completed (page 3 lines 5-8). See also page 3 lines 5-10.

As to claim 6, AAPA discloses the invention as claimed above. AAPA further discloses the first requester issues multiple requests (page 2 line 1, multiple tasks), and wherein the circuit prevents any further instruction processing from occurring within the first requester until all invalidation operations have been completed (page 2 lines 23-30) for all of the multiple requests.

As to claim 7, AAPA discloses the invention as claimed above. AAPA further discloses the first requester is a processing node (page 1 lines 28-29) that includes multiple processors, wherein the circuit resides within one of the multiple processors and includes logic to execute an instruction to stall the processor until all of the invalidation operations have been completed for data previously provided to the processor (page 2 lines 28-31 and page 3 lines 5-8).

As to claim 8, AAPA discloses the invention as claimed above. AAPA further discloses the first requester is a processing node (page 1 lines 28-29) that includes multiple processors, wherein the circuit resides within one of the multiple processors and includes logic to execute an instruction to stall the processor until all of the invalidation operations have been completed for data previously provided to predetermined ones of the processor in the processing node (page 2 lines 28-31 and page 3 lines 5-8).

As to claim 19, AAPA discloses a system for use in managing requests within a data processing system (page 1 lines 28-30), comprising: means for providing data in response to a request before all read-only copies of the data that reside within the data processing system at the time of receipt of the request have been invalidated (page 3 lines 1-3); and means for selectively discontinuing predetermined data processing tasks until all of the read-only copies have been invalidated (page 2 lines 23-30).

As to claim 20, AAPA discloses the invention as claimed above. AAPA further discloses wherein the data processing system includes a shared main memory (Page 1 lines 29-30) coupled to multiple instruction processors (page 1 lines 29-30), and wherein the means for selectively stalling includes means provided within at least one of the instruction processors for executing a predetermined instruction to stall the at least one instruction processor (page 2 lines 29-30).

As to claim 21, AAPA discloses the invention as claimed above. AAPA further discloses wherein the means for executing includes means for stalling (page 2 lines 29-30) the respective instruction processor until all read-only copies of any data that was previously requested by the instruction processor have been invalidated .

As to claim 22, AAPA discloses the invention as claimed above. AAPA further discloses wherein execution of the predetermined instruction by a instruction processor issues a request for data, and wherein the means for selectively stalling (page 2 lines 29-30) includes request tracking means for delaying return of the data until all read-only copies of any data that was previously requested by the instruction processor have been invalidated (page 3 lines 1-10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 9-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) pages 1-3 in view of Chiou et al. (Chiou) US Patent No. 6,792,507.

As to claim 2, AAPA discloses the invention as claimed above. However, AAPA does not specifically disclose the data is provided before the invalidation operations are completed.

Chiou discloses the data is provided before the invalidation operations are completed (Col. 15 lines 4-8) for the purpose of providing capability of critical and noncritical coherent modes of operation (col. 15 lines 1-33) thereby increasing system bandwidth by proving data first in the noncritical coherent mode.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the data is provided before the invalidation operations are completed as taught by Chiou into the system of AAPA for the advantages stated above.

As to claim 9, AAPA discloses for use in a system having multiple requesters (page 1 lines 28-30) coupled to a shared memory (page 1 lines 29-30), a method for controlling processing of requests, comprises issuing a request (page 2 lines 24-26) for data by a requester to the shared memory; and stalling the requester until all of the read-only copies have been invalidated (pag2 lines 29-30, delaying reads on this limitation and page 3 lines 5-8). However, AAPA does not specifically disclose providing the data from the shared memory in response to the request

before all read-only copies of the data retained by other requesters have been invalidated.

Chiou discloses providing the data from the shared memory in response to the request before all read-only copies of the data retained by other requesters have been invalidated (col. 15 lines 4-8) for the purpose of providing capability of critical and noncritical coherent modes of operation (col. 15 lines 1-33).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate providing the data from the shared memory in response to the request before all read-only copies of the data retained by other requesters have been invalidated as taught by Chiou into the system of AAPA for the advantages stated above.

As to claim 10, AAPA and Chiou disclose the invention as claimed above. AAPA further discloses the initiation by the requester of a hardware sequence to stall the requester until the read-only copies have been invalidated (page 2 lines 23-30).

As to claim 11, AAPA and Chiou disclose the invention as claimed above. AAPA further discloses the requester is an instruction processor (page 1 line 29), and further including execution of a predetermined instruction to initiate the hardware sequence (page 3 lines 4-5, ordered request).

As to claim 12, AAPA and Chiou disclose the invention as claimed above.

AAPA further discloses the instruction is part of the hardware instruction set of the instruction processor (page 1 lines 29-30).

As to claim 13, AAPA and Chiou disclose the invention as claimed above. AAPA further discloses including repeating steps a.) and b.) for multiple requests (pag1 lines 29-30 and page 2 line 1), and stalling the requester until all read-only copies of any data requested by any of the multiple requests have been invalidated (page 2 lines 23-30). Duncan further discloses including multiple requests (col. 3 lines 43-47).

As to claim 14, AAPA and Chiou disclose the invention as claimed above. AAPA further discloses the requester is a processing node containing multiple processors (page 1 lines 28-30), and wherein the method for controlling processing of requests, comprises issuing a request (page 2 lines 24-26) for data by a requester to the shared memory; and stalling the requester until all of the read-only copies have been invalidated (pag2 lines 29-30, delaying reads on this limitation and page 3 lines 5-8). However, AAPA does not specifically disclose providing the data from the shared memory in response to the request before all read-only copies of the data retained by other requesters have been invalidated.

Chiou further discloses providing the data from the shared memory in response to the request before all read-only copies of the data retained by other requesters have been invalidated (col. 15 lines 4-8) for the purpose of providing capability of critical and noncritical coherent modes of operation (col. 15 lines 1-33).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate providing the data from the shared memory in response to the request before all read-only copies of the data retained by other requesters have been invalidated as taught by Chiou into the system of AAPA for the advantages stated above.

As to claim 15, AAPA and Chiou disclose the invention as claimed above. AAPA further discloses including repeating steps a.) and b.) for multiple requests (pag1 lines 29-30 and page 2 line 1), and c) stalling the requester until all read-only copies of any data requested by any of the multiple requests have been invalidated (page 2 lines 23-30). Duncan further discloses including multiple requests (col. 3 lines 43-47).

As to claim 16, AAPA and Chiou disclose the invention as claimed above. AAPA further discloses wherein steps a.) through c.) may be performed for more than one processor (Page 1 lines 29-30) in the processing node, and wherein step c.) comprises stalling a processor until all read-only copies of any data previously provided to the processor have been invalidated (page 2 lines 23-30).

As to claim 17, AAPA and Chiou disclose the invention as claimed above. AAPA further discloses wherein steps a.) through c.) may be performed for more than one processor (Page 1 lines 29-30) in the processing node, and wherein step c.) comprises stalling a processor until all read-only copies of any data previously

provided to predetermined ones of the processors in the processing node have been invalidated (page 2 lines 23-30).

As to claim 18, AAPA and Chiou disclose the invention as claimed above. AAPA further discloses issuing an inter-processor interrupt by the requester to another requester to indicate that data stored within the shared memory by the requester may be accessed by the other requester (col. 7 lines 43-62, response channel and assuming access to the data is permitted read on this limitation).

6. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) pages 1-3 in view of Chiou et al. (Chiou) US Patent No. 6,792,507 and further in view of Duncan et al. (Duncan) US Patent No. 6,647,453.

As to claim 3, AAPA and Chiou disclose the invention as claimed above. However, neither AAPA nor Chiou specifically discloses the memory circuit includes a request channel and a response channel.

Duncan discloses the memory circuit includes a request channel (col. 7 lines 50-51) and a response channel (col. 7 lines54-55) for the purpose of increasing bandwidth by providing separate channel.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the memory circuit includes a request

channel and a response channel by Duncan into the combined invention of AAPA and Chiou for the advantages stated above.

As to claim 4, AAPA, Chiou and Duncan disclose the invention as claimed above. Duncan further discloses the memory circuit includes an acknowledge tracker (col. 7 line 60) to initiate the transfer of an acknowledge to the first requester when all invalidation operations for the requested data are completed.

As to claim 5, AAPA, Chiou, and Duncan disclose the invention as claimed above. Duncan further discloses the requester includes a request tracking circuit responsively coupled to the memory to record when the acknowledge is outstanding for the requested data.

Response to Amendment

7. Applicant's arguments filed on 10/13/05 have been fully considered but they are not deemed to be persuasive.

Applicant's remarks that the references not teaching a circuit included within the first requester and responsively coupled to the memory circuit to execute an instruction that causes the first requester to temporarily enter a stalled state until all of the invalidation operations have been completed is not considered persuasive.

AAPA discloses a circuit (page 2 line 23, cache coherency reads on this limitation, since it requires a logic circuitry to execute method logically. Also see page 3

line 13, logic and line 16, methodology) included within the first requester and responsively coupled to the memory circuit to execute an instruction that causes the first requester to temporarily enter a stalled state (pag2 lines 24-30, "delaying processing" and "invalidating old copies of data before data is provided to an IP" read on this limitation) until all of the invalidation operations have been completed (page 3 lines 5-8). In other words, page 2 lines 24-30 and page 3 line 11-18 discloses the above limitations, since cache coherency requires a logic circuitry to execute coherency method logically and since the first IP request is delayed while invalidating old copies than data is provided to the requested IP. Page 3 lines 5-10, also discloses that invalidation must be completed before providing data to the request IP for the purpose of maintaining data coherency.

Therefore broadly written claims are disclosed by the references cited.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong C Kim whose telephone number is 703-305-3835. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:
(703) 872-9306

H Kim
Primary Patent Examiner
November 20, 2005